**In The Claims:**

1. (Currently Amended) A memory module for operation in a data memory system, comprising:

a plurality of data memory devices for storing ~~useful~~ data, wherein the data memory devices are configured as DRAM modules;

at least one buffer device connected to the data memory devices by at least ~~via~~ data lines, and serving to condition at least data signals, the data signals being transferred on the data lines between the data memory devices and a memory control ~~checking~~ device of the data memory system; and

at least one buffer and error checking module, which in each case integrates a buffer device and a data memory device for storing redundancy data operable to detect and to correct erroneous data in a common device housing.

2. (Currently Amended) The memory module of claim 1, wherein each of the buffer and error checking modules is connected to an even number of data memory devices for storing the ~~useful~~ data.

3. (Original) The memory module of claim 2, wherein the data memory devices are arranged symmetrically with respect to the buffer and error checking module.

4. (Currently Amended) The memory module of claim 1, wherein the buffer and error checking module has an error detecting unit operable to perform the following: [[,]]

during a transfer of ~~useful~~ data to the memory module, to form and to store the redundancy data; and [[,]]

during a transfer of ~~useful~~ data to the memory control ~~checking~~ device, to form check data from the ~~useful~~ data ~~to be transferred~~ and also to compare respectively corresponding redundancy data ~~and~~ with the check data.

5. (Currently Amended) The memory module of claim 4, wherein the buffer and error checking module has an error correction unit operable to correct erroneous ~~useful~~ data on the basis of respectively corresponding redundancy data and check data.

6. (Currently Amended) The memory module of claim 5, wherein ~~the memory module is absent a contact device assigned to a data line for transferring redundancy data~~ any error correction is performed exclusively on the memory module and without communication with the memory control device.

7. (Currently Amended) The memory module of claim 5, wherein the memory module has an error signaling unit operable to transfer information on error events to the memory control ~~checking~~ device.

8. (Original) The memory module of claim 5, wherein the buffer and error checking module has an error evaluation unit operable to identify and to mask out defective memory cells in the data memory devices.

9. (Canceled)

10. (Original) The memory module of claim 1, wherein the data memory devices comprise a DDR interface.

11. (Original) The memory module of claim 1, wherein the maximum dimensions of the memory module are about 1.2 inches x 5.25 inches.

12. (Currently Amended) A buffer and error checking module for memory modules, the memory modules comprising in each case a plurality of DRAM devices operated in data memory systems, the buffer and error checking module comprising:

connecting devices;

a buffer/redriver formed in a semiconductor substrate and operable to condition at least data signals that are transferred to and from the memory modules; and

a memory cell array formed in the semiconductor substrate as an error data memory.

13. (Currently Amended) The buffer and error checking module of claim 12, further comprising an error detecting unit operable, during a transfer of ~~useful~~ data to the memory module, to form and to store redundancy data and, during a transfer of ~~useful~~ data to a memory control ~~checking~~ device of the data memory system, to compare the stored redundancy data with check data formed from the ~~useful~~ data to be transferred.

14. (Currently Amended) The buffer and error checking module of claim 13, further comprising an error correction unit operable to correct erroneous ~~useful~~ data on the basis of respectively corresponding redundancy data and check data.

15. (Original) The buffer and error checking module of claims 13, further comprising an error signaling unit operable to transfer information on error events to the data memory system.

16. (Original) The buffer and error checking module of claim 13, further comprising an error evaluation unit operable to identify and to mask out defective memory cells in data memory devices connected to the buffer and error checking module.

17. (Currently Amended) A method for operating a memory module having a plurality of ~~data memory~~ DRAM devices for storing ~~useful~~ data and at least one buffer and error checking module in a data memory system, the method comprising:

receiving data signals of ~~useful~~ data transferred to the memory module and conditioning the data signals with the buffer and error checking module;

forming, in the buffer and error checking module, a corresponding set of redundancy data with respect to the ~~useful~~ data;

storing the ~~useful~~ data in the ~~data memory~~ DRAM devices;

storing the respectively corresponding set of redundancy data in the buffer and error checking module;

forming in the buffer and error checking module, during a transfer of stored ~~useful~~ data from the ~~data memory~~ DRAM devices to a memory control ~~checking~~ device of the data memory system, a corresponding set of check data;

detecting, through a comparison of respectively corresponding redundancy data and check data, data errors that have occurred in the ~~useful~~ data are and correcting any such errors on a case by case basis; and

transferring corrected ~~and essentially error-free useful~~ data to the memory control ~~checking~~ device.

18. (Currently Amended) The method of claim 17, further comprising signaling an occurrence of a data error in the ~~useful~~ data to the memory control ~~checking~~ device of the data memory system.

19. (Currently Amended) The method of claim 17, further comprising optimizing a data memory system by:

providing a redundancy bus system in precursor systems on a system board between a memory control ~~checking~~ device and the memory module;

registering transfer errors in the bus system and analyzing, in the precursor systems, the transfer errors by the memory control ~~checking~~ device with the aid of the redundancy bus system;

developing, on the basis of an analysis of transfer errors occurring between the memory control ~~checking~~ device and the memory module, a bus system of respective precursor systems in a direction of a minimum number of transfer errors; and

providing the data memory system with the bus system developed for a minimum number of transfer errors.

20. (Canceled)